IN THE CLAIMS:

Please amend claims 1, 2 14 and 15, and add new claims 16-18 as follows:

LISTING OF CURRENT CLAIMS

Claim 1. (Currently Amended) A face-to-face multi-chip flip-chip package comprising:

a package substrate having a top surface, a bottom surface and a concave wall between the top surface and the bottom surface, wherein the concave wall defines a chip accommodation space;

a first chip having a first active surface and a first back surface, wherein the first active surface of the first chip faces to the bottom surface of the package substrate;

at least a second chip having a second active surface, a second back surface and a ~~plurality of side surfaces~~ side surface between the second active surface and the second back surface of the second chip, wherein the second active surface of the second chip faces to the first active surface of the first chip, the concave wall is not parallel to the side surface of the second chip; and

an underfilling material formed between the first chip and the second chip.

Claim 2. (Currently Amended) The face-to-face multi-chip flip-chip package of claim 1, wherein the chip accommodation space is an opening passing through the top surface and the bottom surface of the package substrate.

Claim 3. (Original) The face-to-face multi-chip flip-chip package of claim 2, wherein the opening is circular or elliptic shape.

Claim 4. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein a plurality of solder balls are formed on the package substrate.

Claim 5. The face-to-face multi-chip flip-chip package of claim 1, wherein the first chip is a logic chip.

Claim 6. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein the size of the first chip is larger than the size of the chip accommodation space.

Claim 7. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein the second chip is a memory chip.

Clam 8. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein the size of the second chip is smaller than the size of the first chip.

Claim 9. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein the size of the chip accommodation space is smaller than the size of the first chip and larger than the size of the second chip.

Claim 10. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein the second chip is disposed inside the chip accommodation space.

Claim 11. (Original) The face-to-face multi-chip flip-chip package of claim 1, wherein the underfilling material is filled in the chip accommodation space.

Claim 12. (Original) The face-to-face multi-chip flip-chip package of claim 1, further comprising a plurality of first bumps formed between the first chip and the package substrate.

Claim 13. (Original) The face-to-face multi-chip flip-chip package of claim 12, wherein the underfilling material encloses the first bumps.

Claim 14. (Currently Amended) The face-to-face multi-chip flip-chip package of claim 1, wherein ~~the side surfaces of th second chip have a progressive distance from~~ the concave wall is located a progressive distance from the side surface of the second chip.

Claim 15. (Currently Amended) The face-to-face multi-chip flip-chip package of claim 1, wherein the underfilling material is disposed between the side ~~surfaces~~ surface of the second chip and the concave wall.

Claim 16. (New) A face-to-face multi-chip flip-chip package comprising:

a package substrate having a top surface, a bottom surface and a concave wall between the top surface and the bottom surface, wherein the concave wall defines a chip accommodation space, the concave wall is curvilinear;

a first chip having a first active surface and a first back surface, wherein the first active surface of the first chip faces to the bottom surface of the package substrate;

a plurality of first bumps formed between the first chip and the package substrate;

at least a second chip having a second active surface, a second back surface and a side surface between the second active surface and the second back surface of the second chip, wherein the second active surface of the second chip faces to the first active surface of the first chip; and

an underfilling material formed between the first chip and the second chip.

Claim 17. (New) The face-to-face multi-chip flip-chip package of claim 16, wherein the size of the chip accommodation space is smaller than the size of the first chip and larger than the size of the second chip.

Claim 18. (New) The face-to-face multi-chip flip-chip package of claim 16, wherein the concave wall is located a progressive distance from the side surface of the second chip.